IN THE CLAIMS:

Original Claims 1-21 were previously cancelled and new claims 22-49 were previously added. The pending claims were 22-49 and the claims now are as follows:

22. (Currently Amended) An assembly of a ground plane and a semiconductor chip, comprising:

at least one first capacitor plate provided within the semiconductor chip, and at least one second capacitor plate, the first and second capacitor plates being separated by a dielectric layer and capacitively coupled to each other via the dielectric layer, and the ground plane comprising at least one first conducting member and at least one electrically conducting via extending through a supporting member of the semiconductor chip and electrically coupled in series with the second capacitor plate; and wherein

the second capacitor plate comprises a layer of electrically conductive glue which attaches the ground plane to the semiconductor chip.

23. (Currently Amended) An assembly according to claim 22, wherein:

a resonant frequency of the capacitance provided by the first capacitor plate and the second capacitor plate, and an inductance provided by the at least one first conducting member, is approximately equal to an intended working frequency of the chip.

24. (Currently Amended) An assembly according to claim 22, wherein:

the dielectric layer is an integral part of the chip.

25. (Currently Amended) An assembly according to claim 23, wherein:

the dielectric layer is an integral part of the chip.

26. (Currently Amended) An assembly according to claim 24, wherein:

the dielectric layer is an outer surface of the chip facing the supporting member.

27. (Currently Amended) An assembly according to claim 25, wherein:

the dielectric layer is an outer surface of the chip facing the supporting member.

28. (Currently Amended) An assembly according to claim 24, wherein:

the dielectric layer comprises silicon oxide.

29. (Currently Amended) An assembly according to claim 25, wherein:

the dielectric layer comprises silicon oxide.

30. (Currently Amended) An assembly according to claim 22, wherein:

the second capacitor plate comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

31. (Currently Amended) An assembly according to claim 23, wherein:

the second capacitor plate comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

32. (Currently Amended) An assembly according to claim 23 wherein:

the second capacitor plate comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

33. (Currently Amended) An assembly according to claim 23, wherein:

the second capacitor plate comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

34. (Currently Amended) An assembly according to claim 23, wherein:

the second capacitor plate comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

35. (Currently Amended) An assembly according to claim 23, wherein:

the second capacitor plate comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

36. (Currently Amended) An assembly according to claim 23, wherein:

the second capacitor plate comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

37. (Currently Amended) An assembly according to claim 23, wherein:

the second capacitor plate comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

Claims 38-45 are cancelled without disclaimer or prejudice.

46. (Currently Amended) An assembly according to claim 22, wherein:

the at least one electrically conducting via extending through the supporting member is directly connected to the second capacitor plate.

47. (Currently Amended) An assembly according to claim 30, wherein:

the vias and the metallic layer are integrally formed from a same metal.

48. (Currently Amended) A method of assembly of a ground plane and a semiconductor chip mounted on a supporting member of a chip containing a first capacitor plate and a dielectric coating, comprising providing the ground plane on a metal covered area on a surface of the supporting member, providing vias electrically connected to the metal covered area and extending therefrom through the supporting member to the opposite side thereof, connecting in parallel at least two of the vias which provide an inductance and are coupled to the ground plane, and using an electrically conductive glue between the chip and the metal covered area to attach the metal covered area to the chip.

49. (Currently Amended) A semiconductor chip package comprising:

a semiconductor chip containing a first capacitor plate and a dielectric coating and a supporting member, the supporting member comprising at least one metal covered area which is a ground plane and at least one electrically conductive via extending from the metal covered area through the supporting member which provides an inductance and are coupled to the ground plane, and wherein the chip is adhered to the supporting member by means of an electrically

conductive glue and the electrically conductive glue is in electrical contact with the metal covered area and the electrically conductive glue is a second capacitor plate and the first and second capacitor plates and the dielectric form a capacitor and the capacitance and inductance comprise a series circuit coupling the capacitance to ground.